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Francis I. Gray
TEKTRONIX, INC.
MS 50-LAW
P.O. Box 500
Beaverton, OR 97077

EXAMINER	
DAMIANO, ANNE L	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/912,806	GERNHARDT, BIRGER	
	Examiner	Art Unit	
	Anne L Damiano	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 7/19/04. These drawings are acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 3-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Dorsey et al. (6,198,751).

As in claim 1, Dorsey discloses a device for analyzing digital data formulated in accordance with a communication protocol, comprising:

a) a data memory *(input memory)* for storing the digital data to be analyzed *(column 4: lines 45-49); (Data that is translated is analyzed in the translation process.)*

b) a microcode memory *(microcoded control unit)* for storing a microcode that represents at least part of the communication protocol *(column 2: lines 42-45, column 8: lines 2-5)*;

c) a data register for reading out a pre-determined number of bits from the data memory *(column 8: lines 2-12); (When the packet in the data memory is translated, it's content will be loaded to a register in the translator control unit.)*

d) a microcode register for reading out a pre-determined number of bits from the microcode memory, with the content of the microcode register being usable for analyzing the content of the data register *(column 2: lines 43-45 and column 8: lines 11-19)*;

e) an output memory into which the results of the analysis are entered *(column 2: lines 19-26)*;

f) a first addressing unit for addressing the data memory *(address control of the input memory) (column 7: lines 22-24 and figure 5: component 53b)*; and

g) a second addressing unit for addressing the microcoded memory *(address control that sets start place for the translation process) (column 2: lines 56-58, column 8: lines 13-19 and figure 5: component 51b)*, with the first and second addressing units being designed to take into account the content of the data register and/or the microcode register when subsequent addresses are determined *(column 8: lines 5-31 and figure 5: component 53b, 53a, 58 and 59) (The addressing units control the writing to the output memory including its associated address control by taking into account the content of the input memory and the microcoded translation instructions. Since this process is occurring sequentially (column 2: lines 56-58), the address to which the data is written in the output memory is subsequent or following the addresses of the data memory and microcoded memory.)*

As in claim 3, Dorsey discloses the device according claim 1 wherein the data register is designed to align and/or shift its content *(alignment units) (column 12: lines 20-37).*

As in claim 4, Dorsey discloses a device according to claims 1 or 3 further comprising a register block *(Figure 5-not labeled with a component number but labeled as ADDRESS CONTROL for OUTPUT MEM (component 58))*, with at least one register and at least one counter *(clock)* the contents of which are taken into account for determining the subsequent addresses for the first and second addressing units, the at least one register being and the at least one counter being used to take into account the contents of the data register and/or the microcode register. *(column 8: lines 5-31 and figure 5: component 53b, 53a, 58, 59 and (not labeled with a component number but labeled as ADDRESS CONTROL for OUTPUT MEM (component 58)). (The addressing units control the writing to the output memory including its associated address control by taking into account the content of the input memory and the microcoded translation instructions. Since this process is occurring sequentially (column 2: lines 56-58), the address to which the data is written in the output memory is subsequent or following the addresses of the data memory and microcoded memory. The writing to the output memory involves the utilization of the address control (not labeled with a component number but labeled as ADDRESS CONTROL of fig 9 for OUTPUT MEMORY (component 97)). The address control is a register and includes a clock, which is a counter and is considered or taken into account when determining the subsequent addresses.)*

As in claim 5, Dorsey discloses the device according to claim 4 (as dependent on claim 1 or 3) further comprising a third addressing unit for the output memory *(Figure 5-not labeled with a component number but labeled as ADDRESS CONTROL for OUTPUT MEM (component 58))*, with the address of the third addressing unit being changeable by taking the content of the microcode register into account *(The writing to the output memory involves the utilization of the address control (not labeled with a component number but labeled as ADDRESS CONTROL of fig 9 for OUTPUT MEMORY (component 97). The addressing units control the writing to the output memory including its associated address control by taking into account the content of the input memory and the microcoded translation instructions.)*

As in claim 6, the device according to claim 5 (dependent on claim 4, as dependent on claim 1 or 3) further comprising a logic circuit with which an entry into the output memory is read out, changed to take into account a new result, and rewritten into the output memory *(column 8: lines 24-31)*.

As in claim 7, Dorsey discloses the device according to claim 6 (dependent on claim 5, that is dependent on claim 4, as dependent on claim 1 or 3) wherein a starting address is loaded into the addressing units *(column 7: lines 22-24 and column 8: lines 17-19)*.

As in claim 8, Dorsey discloses The device according to claim 7 (dependent on claim 6, that is dependent on claim 5, that is dependent on claim 4 as dependent on claim 1 or 3) where the digital data to be analyzed are protocol data units that contain parameters; and the results

entered into the output memory have at least one parameter identifier and at least one parameter value *(translated headed) (The output has a header that includes information identifying the network protocol. This information identifying the protocol is equivalent to parameters.) (column 4: line 66-column 5: line 10 and column 7: lines 29-35).*

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey as applied to claim 1 above.

Regarding claim 2, Dorsey discloses the device for analyzing digital data with first and second addressing unit above. However, Dorsey does not specifically disclose each addressing unit comprising a counter that may be changed in accordance with the content of the data register and/or microcode register when the subsequent addresses are determined.

It would have been obvious to a person skilled in the art at the time the invention was made to include a counter in the addressing units in the system taught by Dorsey. It would have been obvious because a person skilled in the art would understand, that although not specifically

disclosed, Dorsey's addressing units have address counters that change in accordance with the content of the data registers when the subsequent address are determined and are used when reading from the registers.

As in claim 4, Dorsey discloses a device according to claim 2 further comprising a register block *(Figure 5-not labeled with a component number but labeled as ADDRESS CONTROL for OUTPUT MEM (component 58)),* with at least one register and at least one counter *(clock)* the contents of which are taken into account for determining the subsequent addresses for the first and second addressing units, the at least one register being and the at least one counter being used to take into account the contents of the data register and/or the microcode register. *(column 8: lines 5-31 and figure 5: component 53b, 53a, 58, 59 and (not labeled with a component number but labeled as ADDRESS CONTROL for OUTPUT MEM (component 58)). (The addressing units control the writing to the output memory including its associated address control by taking into account the content of the input memory and the microcoded translation instructions. Since this process is occurring sequentially, the address to which the data is written in the output memory is subsequent or following the addresses of the data memory and microcoded memory. The writing to the output memory involves the utilization of the address control (not labeled with a component number but labeled as ADDRESS CONTROL of fig 9 for OUTPUT MEMORY (component 97)). The address control is a register and includes a clock, which is a counter.)*

As in claim 5, Dorsey discloses the device according to claim 4 (as dependent on claim 2) further comprising a third addressing unit for the output memory *(Figure 5-not labeled with a component number but labeled as ADDRESS CONTROL for OUTPUT MEM (component 58))*, with the address of the third addressing unit being changeable by taking the content of the microcode register into account *(The writing to the output memory involves the utilization of the address control (not labeled with a component number but labeled as ADDRESS CONTROL of fig 9 for OUTPUT MEMORY (component 97). The addressing units control the writing to the output memory including its associated address control by taking into account the content of the input memory and the microcoded translation instructions.)*

As in claim 6, the device according to claim 5 (dependent on claim 4, as dependent on claim 2) further comprising a logic circuit with which an entry into the output memory is read out, changed to take into account a new result, and rewritten into the output memory *(column 8: lines 24-31)*.

As in claim 7, Dorsey discloses the device according to claim 6 (dependent on claim 5, that is dependent on claim 4, as dependent on claim 2) wherein a starting address is loaded into the addressing units *(column 7: lines 22-24 and column 8: lines 17-19)*.

As in claim 8, Dorsey discloses The device according to claim 7 (dependent on claim 6, that is dependent on claim 5, that is dependent on claim 4 as dependent on claim 2) where the digital data to be analyzed are protocol data units that contain parameters; and the results entered

into the output memory have at least one parameter identifier and at least one parameter value *(translated headed) (The output has a header that includes information identifying the network protocol. This information identifying the protocol is equivalent to parameters.) (column 4: line 66-column 5: line 10 and column 7: lines 29-35).*

Regarding claim 9 (dependent on claim 8, that is dependent on claim 7, that is dependent on claim 6, that is dependent on claim 5, that is dependent on claim 4 as dependent on claim 1, 2 or 3), Dorsey discloses the claim invention except for the memories being combined in one physical memory and the corresponding address units being combined in one physical addressing unit.

It would have been obvious to a person skilled in the art at the time the invention was made to combine the memories in one physical memory and one physically addressing unit, since it is held that rearranging parts of an invention involves only routine skill in the art.

6. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dorsey et al. (6,198,751).

Regarding claim 10, Dorsey discloses a method of analyzing digital data formulated in accordance with a communication protocol comprising the steps of:

a) loading the digital data to be analyzed into a data memory *(input memory) (column 4: lines 45-49); (Data that is translated is analyzed in the translation process.)*

b) loading a microcode into a microcode memory *(microcoded control unit),* with the microcode representing at least part of the communication protocol *(column 2: lines 42-45, column 8: lines 2-5)*;

c) reading out a pre-determined number of bits from the data memory into a data register in accordance with an address specified by a first addressing unit *(column 8: lines 2-18,); (When the packet in the data memory is translated, it's content will be loaded to a register in the translator control unit.)*

d) reading out a pre-determined number of bits from the microcode memory into a microcode register in accordance with an address specified by a second addressing unit *(column 2: lines 43-45 and column 8: lines 11-19)*;

e) Assigning functions to the data bits in the data register according to the bits in the microcode register *(column 2: lines 19-26); (Translating from one protocol to another involves assignment of objects or functions to the data bits in the data register. The microcode register holds the different sets of microcode for the different communications protocols and so the assigning happens in accordance with the bits in the microcode register.)*

f) entering at least one result of the assignment in an output memory *(column 2: lines 19-26).*

Dorsey discloses the address control unit causing a jump in the address being read from the data memory *(column 10: lines 58-65).* However, Dorsey does not specifically disclose updating counter reading for the first and second addressing units in accordance with the contents of the data register and/or the microcode register.

It would have been obvious to a person skilled in the art at the time the invention was made to include a counter in the addressing units in the system taught by Dorsey. It would have been obvious because a person skilled in the art would understand, that although not specifically disclosed, Dorsey's addressing units have address counters that change in accordance with the content of the data registers and are used when reading from the registers.

Regarding claim 11, Doresy discloses the method according to claim 10 wherein the entry in accordance with step f) takes place at an address specified by a third addressing unit *(figure 5: component 58 and adjacent address control and column 8: lines 27-31).*

However, Dorsey does not specifically disclose a counter reading for the third addressing unit being updated in accordance with the content of the microcode register.

It would have been obvious to a person skilled in the art at the time the invention was made to include a counter in the addressing units in the system taught by Dorsey. It would have been obvious because a person skilled in the art would understand, that although not specifically disclosed, Dorsey's addressing units have address counters that change in accordance with the content of the data registers and are used when reading from the registers.

Regarding claim 12, Dorsey discloses the method according to claim 11 as possibly further including error detection or correction means *(column 7: lines 38-42).* However, Dorsey does not specifically disclose prior to entry in accordance with step f) an incomplete entry is read out from the output memory by a logic circuit and changed to take into account a new result, and then rewritten into the output memory.

It would have been obvious to a person skilled in the art at the time the invention was made to change an incomplete entry to a new result prior to entering it to the output memory in the system taught by Dorsey. It would have been obvious because Dorsey discloses error detection and correction. A person skilled in the art would have understood error correction as being replacing a faulty entry with a correct entry.

As in claim 13, Dorsey discloses the method according to claims 10, 11 or 12 comprising in a further step a register block containing at least one counter which is loaded with the results of the analysis and which are taken into account when subsequent addresses are determined for the first and second addressing units *(column 8: lines 5-31 and figure 5: component 53b, 53a, 58 and 59; The addressing units control the writing to the output memory including its associated address control by taking into account the content of the input memory and the microcoded translation instructions. Since this process is occurring sequentially (column 2: lines 56-58), the address to which the data is written in the output memory is subsequent or following the addresses of the data memory and microcoded memory.)*

Response to Arguments

7. Applicant's arguments filed 7/19/04 have been fully considered but they are not persuasive.

Regarding the first aspect of arguments, the process of translation surely involves analysis.

The content of the data register and/or microcode are used in the translation process of Dorsey. Such data is also used by the controller, which selects data to be written to the output memory including the associated address control *(column 8: lines 25-31)*. Since this process is occurring sequentially *(column 2: lines 56-58)*, the address to which the data is written in the output memory is subsequent or following the addresses of the data memory and microcoded memory. See above claim rejection for further detail.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (571) 272-3658. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALD

SCOTT BADERMAN
PRIMARY EXAMINER